IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

REDSTONE LOGICS LLC, - *Plaintiff*, v. QUALCOMM INC. and QUALCOMM TECHNOLOGIES, INC. - *Defendants*.	§ § § § § § § § § § §	Case. No. 7:24-cv-00231-ADA-DG

DEFENDANTS QUALCOMM INCORPORATED'S AND QUALCOMM TECHNOLOGIES, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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B	ON Semiconductor's application note AND8248/D (*Stys*)
C	U.S. Patent No. 7,538,625 (*Cesky*)
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[1] Exhibits A through H are exhibits to the April 4, 2025 Declaration of Dr. John Villasenor In Support of Defendants' Opening Claim Construction Brief (Ex. 1).

I. INTRODUCTION

The Asserted Claims of U.S. Patent No. 8,549,339 (the "'339 Patent")[2] generally relate to a "multi-core processor" where first/second "set[s] of processor cores" are each "configured to dynamically receive" a corresponding first/second "clock signal" and "supply voltage." *See,* e.g., '339 Patent, Cl. 1. But the claims do not broadly cover all such arrangements. Rather, to obtain allowance, each asserted independent claim was amended to further require, among other things, that "the first clock signal ***is independent*** from the second clock signal" (the "Independent Term," *see infra*, Section IV.A), as shown below:[3]

> 1. A multi-core processor, comprising:
>
> a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
>
> a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and ***the first clock signal is independent from the second clock signal***; and
>
> an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

'339 Patent, Cl. 1 (underline denoting prosecution amendments; Independent Term in bold/italics).

In a related proceeding, Plaintiff Redstone Logics LLC ("Redstone") contended that "the applicant made it clear that the use of 'independent' is best understood as ***simply meaning 'different.'"*** Ex. 2 at 2; *see also id.* at 7 (contending that if "'***independent***' needs clarification"

[2] The '339 Patent is Dkt. 1-1 and is also attached as Ex. A to the April 4, 2025 Declaration of Dr. John Villasenor In Support of Defendants' Opening Claim Construction Brief.
[3] All emphases added unless otherwise noted.

then "it ***merely means 'different.'"***). Qualcomm agrees that this language requires different signals, but both the plain and ordinary meaning and intrinsic record require more than "merely" different signals. First, in a simple hypothetical system described further below, two clock signals can be "different"—but not "independent." This confirms that those terms are not synonymous in this context and that replacing "independent" with "different" as Plaintiff urges improperly alters and broadens the plain meaning.

Second, during prosecution and in response to a rejection, the applicant asserted: "In addition, [in the claims] ***the first clock signal is independent from the second clock signal***. **Instead**, *Kim* discloses the apparatus comprising a multi-core processor [] having ***a single clock source***." Ex. H (Applicant's Resp.) at 10–11. As discussed below, *Kim*[4] discloses exactly what Plaintiff seeks to include and the applicant distinguished—a clock system with two ***different*** clock signals fed from a "***single*** clock source." Having clearly and unequivocally stated that arrangement was not good enough to meet "independent," Federal Circuit law requires holding Redstone to the applicant's public statement. Moreover, Redstone's excuses—this was just one of multiple distinctions and the applicant did not need to say what it said—are each insufficient as a matter of law under Federal Circuit precedent. Accordingly, Qualcomm's construction should be adopted.

Separately, certain dependent Asserted Claims are also invalid because they are indefinite. Specifically, certain dependent Asserted Claims describe the location of structures using terms that do not refer to any particular location or provide any guidance on the metes and bounds of any such region (*i.e.*, "in a ***periphery*** of the multi-core processor" (claim 5) and "in a ***common region*** that is ***substantially central*** to the first set of processor cores and the second set of processor cores" (claim 14)). In the related proceeding, the Magistrate Judge correctly determined that the

[4] As used herein, "*Kim*" refers to U.S. Pat. App. Pub. No. 2009/0138737.

"substantially central" claims are indefinite, but, respectfully, erred in determining that the "periphery" claims are not indefinite.

II. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at or around the relevant time of the alleged invention would have had at least a bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field, as well as at least 2 years of academic or industry experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent. A POSITA with a higher level of education may have fewer years of academic or industry experience, or vice versa. Ex. 1, Declaration of Dr. John Villasenor Regarding Claim Construction ("Villasenor Decl.") at ¶ 25.

III. OVERVIEW OF THE '339 PATENT

The '339 Patent relates to an arrangement of clock and voltage sources supplied to different groups of processor cores in a multi-core processor. '339 Patent at Abstract; 1:61-2:40. The '339 Patent explains that prior art multi-core processors required that "[e]ach processor core in a conventional multi-core processor generally shares the same supply voltage and clock signal to simplify the interfaces between the processor cores." '339 Patent at 1:7-14. To that end, the '339 Patent proposes that each processor core group has an independent power profile powered with a separate supply voltage and that each processor core group obtain a clock output signal from a phase locked loop ("PLL") that receives a clock input signal from an "independent clock domain." *Id.* at 2:27-31, 4:1-17, Fig. 3.

This approach is illustrated below in annotated Fig. 3 of the '339 Patent, which depicts three independent clock signals, "the clock signal 1, the clock signal 2, [and] the clock signal 3" (annotated in green), providing independent inputs to "the respective phase lock loops (PLLs)" 1, 2, and 3. *Id.* at 4:1-17, Fig. 3.

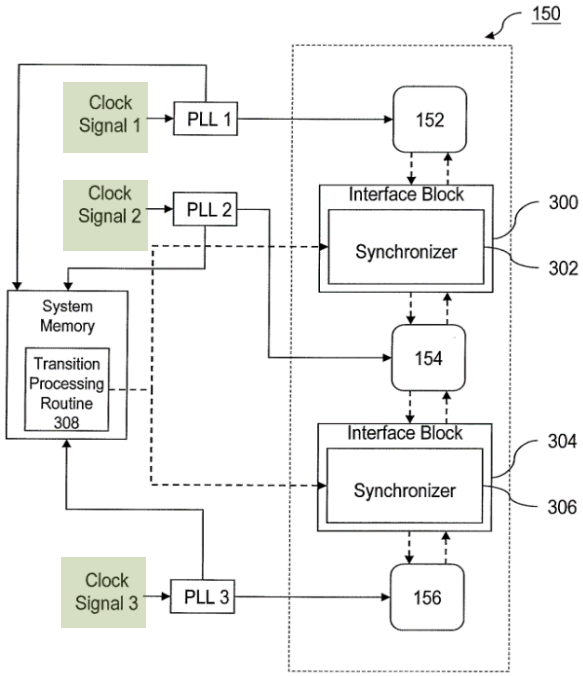


FIG. 3

Id., Fig. 3 (annotated).

Consistent with Fig. 3, each asserted independent claim (claims 1 and 21) of the '339 Patent recites "a first phase lock loop (PLL) having a first clock signal as input" and "a second PLL having a second clock signal as input" wherein "the first clock signal is independent from the second clock signal." *Id.* at claims 1 and 21.

IV. DISPUTED TERMS REQUIRING CONSTRUCTION

A. Term 1: "the first clock signal is independent from the second clock signal"

'339 Patent Claim(s)	Redstone's Proposed Construction	Defendants' Proposed Construction
Claims 1, 21	Plain and ordinary meaning, as urged in the related proceeding, "'independent' is best understood as simply meaning 'different.'" *Redstone Logics LLC v. NXP USA, Inc.*, Case No. 7:24-cv-00028-ADA-DTG, (W.D. Tex., Jan. 8, 2024) ("*NXP Litigation*").	Plain and ordinary meaning, which requires that the first and second clock signals depend from different reference oscillator clocks

The parties agree that this term requires different signals. The principal dispute between the parties is therefore whether the different signals of the Independent Term may originate from a single, shared reference oscillator clock (also known as a clock source), or whether independent clock signals must originate from separate reference oscillator clocks. The plain and ordinary meaning, the knowledge of a POSITA, and the prosecution history each separately dictates not just different clock signals but different clock signals with separate reference oscillator clocks.

1. The plain meaning of "independent" cannot be "different" in the context of clocks in a multicore processor or the '339 Patent's specification

It is axiomatic that two clock signals may be "different" but not "independent," which confirms that Redstone's plain and ordinary meaning of "independent" is incomplete and wrong. Even before considering confirmatory disclaimer and discussions in the intrinsic record, practical examples illustrate why clock signals that are "different" may nevertheless share a dependency.

As background, each core in a multicore processor requires a clock timing reference to operate. Villasenor Decl. at ¶ 35. Before and after the '339 Patent, there were at least two known approaches to generate multiple, ***different*** clock signals to be supplied to components within a

microprocessor. *Id.* at ¶¶ 36-42, 44-46, 50-55. Both approaches begin with the understanding that clock signals typically originate from one or more external reference oscillator clocks. *Id.*

A ***single reference oscillator approach*** may provide multiple different clocks derived from—and ***dependent on***—the same reference oscillator source. *See id.* at ¶ 44. For example, the output of a single reference oscillator clock can be split and its frequency divided or multiplied to create two or more different clock signals having different frequencies (*id.*), as depicted:

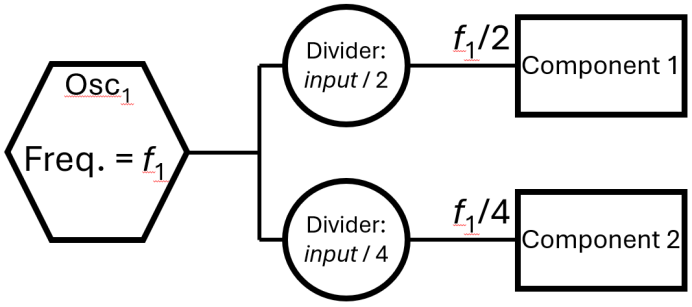


Figure A – Single reference oscillator suppling two components with different frequencies dependent upon single source (Osc_1)

Figure A shows an arrangement where the clock signal from the single reference oscillator (Osc_1) is split and processed by two separate dividers that alter the clock frequency (f_1) generated by the reference oscillator in a fixed manner—here, by one half and one quarter—resulting in an input to Component 1 with a frequency of $f_1/2$ and an input to Component 2 with a frequency of $f_1/4$. *Id.* Clock signals at $f_1/2$ and $f_1/4$ ***do not*** meet the plain and ordinary meaning of "independent" because they remain dependent on the same input, namely clock frequency f_1 provided by reference oscillator Osc_1. *Id.* The frequencies $f_1/2$ and $f_1/4$ are plainly different, yet if the clock frequency (f_1) of the reference oscillator (Osc_1) decreases, the frequencies of the $f_1/2$ and $f_1/4$ clock inputs to Components 1 and 2 will necessarily decrease given their common dependency, *viz.*, reference oscillator Osc_1. *Id.* Even if each divider is variable, the outputs remain dependent on the same common input frequency f_1, such that a change to f_1 causes a change to $f_1/2$ and $f_1/4$. This example demonstrates that two clock signals, such as $f_1/2$ and $f_1/4$, may be different but not independent;

Redstone's attempt to replace "independent" with "different" must be rejected as it does not reflect the plain and ordinary meaning of "independent." Given Redstone's apparent intent to rewrite the claim under the guise of "plain and ordinary meaning," Defendants' proposed clarification of the plain and ordinary meaning is necessary.

During the *NXP Litigation* claim construction hearing, Redstone contended that independence could be generated in the Figure A context by simply unfixing the denominator of the depicted dividers, such that the frequency scaling impact of the dividers could vary and, according to Redstone, introduce independence in the resulting clock signals:

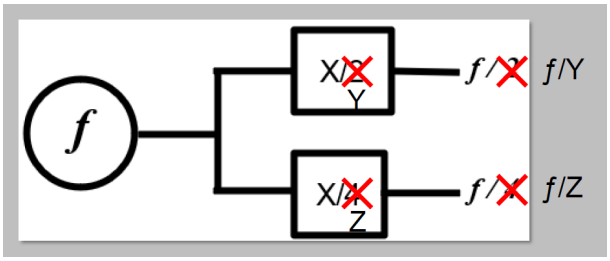


Figure B – Excerpt from Redstone's *Markman* Presentation in the *NXP Litigation*

Ex. 4 at 17; Ex. 5 at 17. Even if two or more factors may affect the frequency of the resulting clock signals, that fails to negate the fact that each of these clock signals remains dependent upon the same reference oscillator. Villasenor Decl. at ¶ 45. As can be seen in Redstone's above image, the resulting clock signals are at frequency *f*/Y and *f*/Z. As in the simplified example above, if the frequency *f* of the reference oscillator were to increase or decrease, so too would the mathematically related frequencies of *f*/Y and *f*/Z—regardless of the values of Y and Z. This is because both clocks are dependent upon clock frequency *f* of the reference oscillator; that is, they are not independent clock signals. *Id.*

A second known approach to generate multiple, different clock signals for use in a microprocessor that existed at the filing of the '339 Patent is a ***multiple reference oscillator approach***—which aligns with the sole approach disclosed in the '339 Patent. *See*, *e.g.*, '339 Patent

at Fig. 3 (depicting "clock signal 1," "clock signal 2," and "clock signal 3" as separate signals); *see also* Villasenor Decl. at ¶ 46. A multiple reference oscillator approach provides multiple clock signals that are ***not dependent*** on the same reference oscillator, as shown:

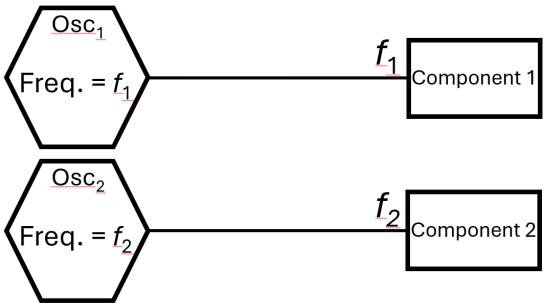


Figure C – Two reference oscillators generating independent clock signals

In this approach, changing the clock frequency f_1 of reference oscillator Osc_1 has no impact on the clock frequency f_2 provided to Component 2. *Id.* And, changing the clock frequency f_2 of reference oscillator Osc_2 has no impact on the clock frequency f_1 provided to Component 1. *Id.* Simply put, when separate reference oscillators are used, the resulting clock signals are independent.

Redstone's previous argument that the single reference oscillator approach (depicted in Figures A and B *supra*) can generate independent clock signals is wrong because it ignores the necessary dependence that exist on the single reference oscillator. Accordingly, its position that "independent" means "simply different" is wrong and contrary to the plain and ordinary meaning of "independent." By contrast, Qualcomm's proposed clarification of the plain and ordinary meaning of the Independent Term that "the first and second clock signals depend from different reference oscillator clocks" is consistent with the plain and ordinary meaning, the knowledge of a POSITA, and the '339 Patent's own Figure 3 disclosure.

2. The prosecution history confirms that the Asserted Claims do not claim two clock signals derived from a single reference oscillator clock

The '339 Patent's file history underscores that the plain and ordinary meaning of the Independent Term is not satisfied with first and second clock signals that are merely "different" as

opposed to signals that are truly "independent." *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (*en banc*) ("the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention"). The applicant distinguished the ***single*** reference oscillator approach from the Independent Term in statements made during prosecution, particularly regarding the *Kim* reference identified by the examiner. These intrinsic record statements confirm that the plain and ordinary meaning of the Independent Term requires "different reference oscillator clocks."

Kim discloses a single reference oscillator configuration, like the example in Figure A, *supra*. Specifically, *Kim* discloses a ***single*** clock source 270 (*i.e.*, a reference oscillator) that feeds a "main PLL 260," which includes "one ***or more frequency dividers***" to generate multiple ***different*** clock signals, as shown by the four colored lines below:

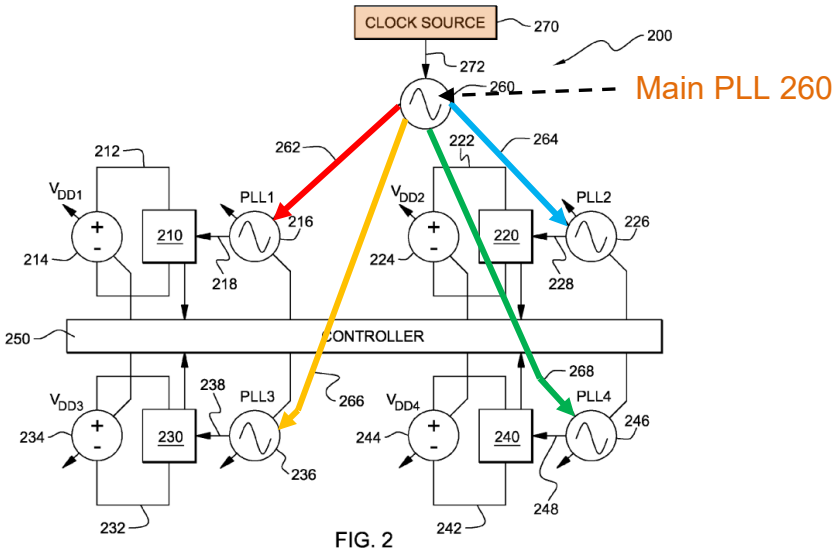


FIG. 2

Ex. E (*Kim*) at Fig. 2 (annotated), [0024]–[0025]; *see also* Villasenor Decl. at ¶¶ 53–54. As with the single reference clock example in Section IV.A.1, *supra*, clock signals 262, 264, 266, and 268 are ***different***, but they are not ***independent*** because they are all multiples of the same original frequency from clock source 270. Villasenor Decl. ¶¶ 54-55. Each of clock signal 262, 264, 266,

and 268 is a separate input to one of PLL 216, 226, 236, or 236. A change to the frequency of clock source 270 will impact each of clock signals 262, 264, 266, and 268, such that they are not independent of each other. *Id.*

During prosecution, the applicant addressed *Kim.* Ex. H at 10-12 (Applicant's Resp.); *see also* Ex. F at 6-9 (Office Action). The applicant made two separate representation, each beginning with "in addition":

File History – Response to Office Action 8/29/2012

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 – 2.

Ex. H (Applicant's Resp.) at 10–11. The second representation makes clear applicants' position: Despite *Kim*'s Figure 2 disclosing clock signals 262 and 264 that are ***different*** based on separate dividers in main PLL 260, that is not good enough to meet the "independent" language because they originate from "a single clock source," namely clock source "270." *Id.* By reciting the "independent" language and distinguishing that language ("[i]nstead") from *Kim's* disclosure of multiple different clock signals fed by a "single clock source," the applicant expressly disclaimed a construction of the Independent Term that would encompass two different signals processed from a single clock source, *i.e.*, an oscillator. This representation forecloses any possibility that "independent" could mean "simply different." The applicant's representation distinguishing *Kim* results in disavowal, as no magic words are required. *See Trs. of Columbia Univ. v. Symantec*

Corp., 811 F.3d 1359, 1364 (Fed. Cir. 2016) (rejecting the "argument that the presumption of plain and ordinary meaning 'can be overcome in only two circumstances: [when] the patentee has ***expressly*** defined a term or has ***expressly*** disavowed the full scope of the claim in the specification and the prosecution history.'" (alteration and emphases in original)).

Redstone may contend here, as it did in the *NXP Litigation*, that the above disclosure should be ignored because the applicant distinguished *Kim* on additional grounds unrelated to its lack of independent clocks, including because *Kim* purportedly did not disclose sets of processor cores. *See* Ex. 2 at 5, 6. This argument does not provide a basis as a matter of law to ignore the applicant's disavowal. As the Federal Circuit has explained, "the scope of surrender is not limited to what is absolutely necessary to avoid a prior art reference; patentees may surrender more than necessary" and "[w]hen this happens, we hold patentees to the actual arguments made, not the arguments that could have been made." *Tech Props. Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1359 (Fed. Cir. 2017); *see also Amgen Inc. v. Coherus Biosciences Inc*., 931 F.3d 1154, 1159 (Fed. Cir. 2019) (noting that "while [the patentee] did assert multiple reasons for why [the prior art] is distinguishable, our precedent instructs that estoppel can attach to each argument"); *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1359 (Fed. Cir. 2017) ("[W]e explained, in the context of disclaimer, that the prosecution history 'includes all express representations made by or on behalf of the applicant to the examiner to induce a patent grant . . . includ[ing] amendments to the claims and arguments made to convince the examiner.'" (some alterations in original, citation omitted)).

The applicant's representations not only amount to a clear disclaimer of a single reference oscillator arrangement, but must also be considered in the context of determining the plain and ordinary meaning of the "Independent Term." This is because prosecution history "may be critical

in interpreting disputed claim terms because it contains the complete record of all the proceedings before the Patent and Trademark Office, including any express representations made by the applicant regarding the scope of the claims." *Personalized Media Commc'ns, LLC v. Apple Inc.*, 952 F.3d 1336, 1340 (Fed. Cir. 2020). "Accordingly, even where prosecution history statements do not rise to the level of unmistakable disavowal, they do inform the claim construction." *Id.* (quotations omitted). "For example, an applicant's repeated and consistent remarks during prosecution can define a claim term by demonstrating how the inventor understood the invention." *Id*. "Similarly, an applicant's amendment accompanied by explanatory remarks can define a claim term by demonstrating what the applicant meant by the amendment." *Id*. And that is exactly what occurred here.

Thus, even if the representations regarding *Kim* did not amount to a disavowal—which they did—they inform the meaning of "independent" clock signals. The applicant used "independent" repeatedly both throughout the response and specific to *Kim* in explaining why the examiner's art was insufficient. And, the applicant separately argued that *Kim* and its multiple different clocks feeding different PLLs was distinguishable because it employed a single clock source. *See* Ex. H at 11 (Applicant's Resp.) ("As discussed above, neither Jacobowitz nor Kim discloses having sets of processor cores ***configured to receive multiple and independent clock signal***."); *id.* at 10–11 (explaining the "***first clock signal is independent from the second clock signal"*** and "***[i]nstead,*** Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having ***a single clock source***"). The applicant chose to use the word "independent," not "different," on multiple occasions in distinguishing *Kim* and other references, and the applicant explained that instead of independent first and second clock signals, *Kim* employed a single clock source, *i.e.*, oscillator 270. Ex. H at 9–11. Thus, the Court should reject

Redstone's "merely different" argument because it is inconsistent with inconsistent with the plain and ordinary meaning of the Independent Term, as confirmed by repeated statements in the prosecution history.

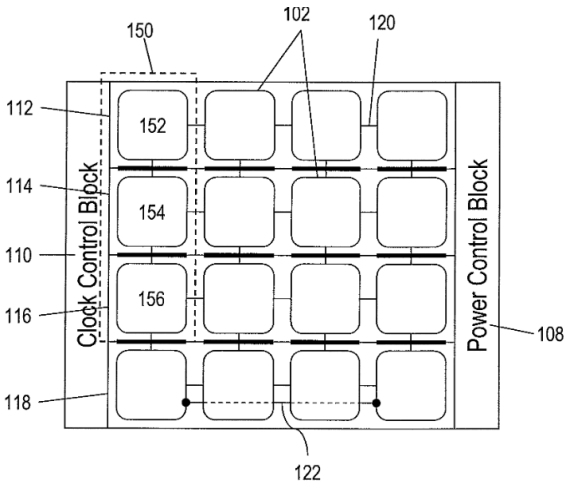
Accordingly, given the parties' clear dispute as to plain and ordinary meaning, and consistent with the intrinsic record, respectfully, the Court should find that the plain and ordinary meaning requires more than merely different clocks but also that the first and second clock signals depend from different reference oscillator clocks. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008) ("plain and ordinary meaning" construction "may be inadequate . . . when reliance on a term's "ordinary" meaning does not resolve the parties' dispute.")

B. Term 2: "located in a periphery of the multi-core processor"

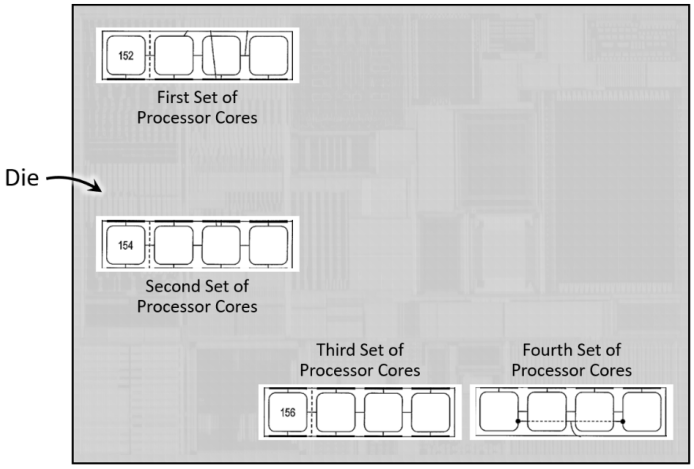
'339 Patent Claim(s)	**Redstone's Proposed Construction**	**Defendants' Proposed Construction**
Claim 5	Plain and ordinary meaning	Indefinite

The term "located in a periphery of the multi-core processor" is indefinite because it fails to inform a POSITA, with reasonable certainty, when a component is "located in a periphery of the multi-core processor" and when it is not. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). This ambiguity results from claim 5's use of the vague term "periphery" coupled with the lack of any required physical relationship between the components of the multi-core processor, which may be spaced apart from each other.

In order to determine whether a "control block[]" is "located in the periphery of the multi-core processor," as claim 5 requires, one must first identify the components of the multi-core processor and their arrangement. The '339 Patent presents a simple example of a multi-core processor with all cores adjacent one another in a grid:



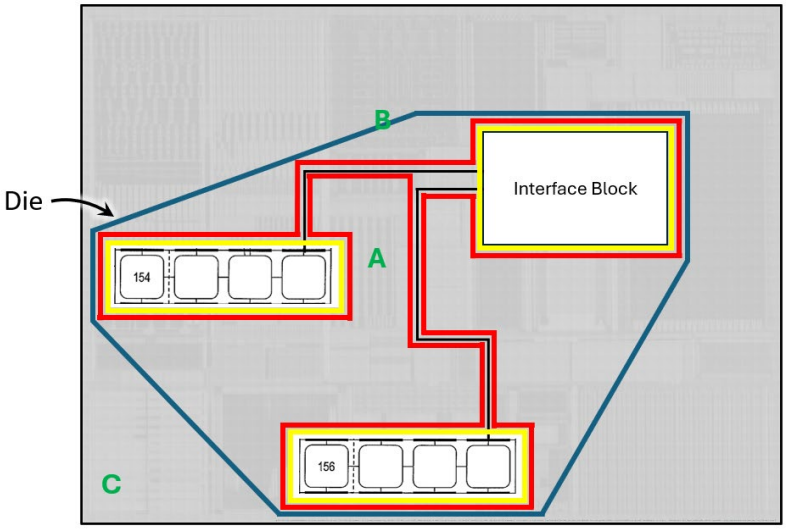
'339 Patent, Figure 1 (excerpt). But the processor cores in the "multi-core processor" of the Asserted Claims need not be arranged in such a grid—nothing within the claims themselves requires a grid arrangement. Villasenor Decl. at ¶ 69. Rather, a POSITA understands that the multiple processor cores may be placed around the semiconductor die, as shown below:



Id. at Figure C; *see also id.* at ¶ 69 ("A POSITA would understand that that the processor cores of a multi-core processor need not be located immediately adjacent to one another in the manner depicted in the patent's Figure 1.").

The below image selects two of the sets of cores and adds the claimed "interface block coupled to the first set of processor cores and also coupled to the second set of processor cores."

See '339 Patent, Cl. 1. The annotation depicts potential "peripheries" in yellow, red, and blue and locations A, B, and C where a control block may be placed:



Villasenor Decl. at Figure G; *see also id.* at ¶¶ 71-72. The yellow "periphery" is actually three separate boundaries, each immediately around a set of cores or the interface block. *Id.* at ¶ 72. The red "periphery" surrounds the same components as well as the circuitry that connects these components. *Id.* And, the blue "periphery" loosely encircles all these components and the other areas of the semiconductor die that lie between the components. *Id.*

But which of these options is the claimed periphery? A POSITA could not know with reasonable certainty, as the term "periphery" is subjective with no commonly understood meaning in the art, and the language of claim 5 provides no guidance to select between the yellow, red, blue, or some other unspecified periphery. *Id.* at ¶¶ 62, 72; *see also id.* at ¶ 68 (noting it is "unclear whether 'periphery of the multi-core processor' might be limited to regions *inside* the multi-core processor within some unspecified distance of the boundary of the multi-core processor, however that boundary might be defined, or whether [it] also includes components outside the multi-core processor but within some unspecified distance of its boundary.").

The '339 Patent's specification does not resolve the uncertainty regarding the scope of periphery. *Id.* at ¶¶ 71, 72. "[P]eriphery" appears only once in the specification: "A power profile associated with an individual processor core may be controlled through signals that may be received from ***control blocks that are located in the periphery*** of the multi-core processor." '339 Patent at 1:62-65. This usage of "periphery" merely parrots claim 5 and offers no additional guidance to a POSITA as to the meaning and scope of "periphery." Villasenor Decl. at ¶ 72.

While the periphery of the simplistic example in Figure 1 of the '339 Patent may be ascertainable, that does not render this claim limitation definite. *See Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1373–74 (Fed. Cir. 2014) ("With this lone example, a skilled artisan is still left to wonder what other forms of [the invention fall within the scope of the claim term]."); *see also Nautilus*, 572 U.S. at 911 ("It cannot be sufficient that a court can ascribe *some* meaning to a patent's claims." (emphasis in original)). Rather, a POSITA seeking to avoid claim 5 of the '339 Patent would not have reasonable certainty in the placement of a control block to ensure they were outside the claim's scope. For example, a control block at reference point B in the above image lies on the blue "periphery," is outside the red "periphery," and is spaced even further from the yellow "periphery." Villasenor Decl. at ¶ 72.

With sets of processor cores and an interface block spaced apart on the semiconductor die—an arrangement that would not be unusual (*id.* at ¶¶ 69-72)—a POSITA could not understand with reasonable certainty what constitutes the "periphery" of such a multi-core processor. *Id.* at ¶¶ 68, 71-73; *see also Nautilus*, 572 U.S. at 901. And, with the location of the periphery not reasonably ascertainable in real world situations, a POSITA cannot know whether a control block is (or is not) "located in a periphery of the multi-core processor." As such, this phrase is indefinite.

C. Term 3: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"

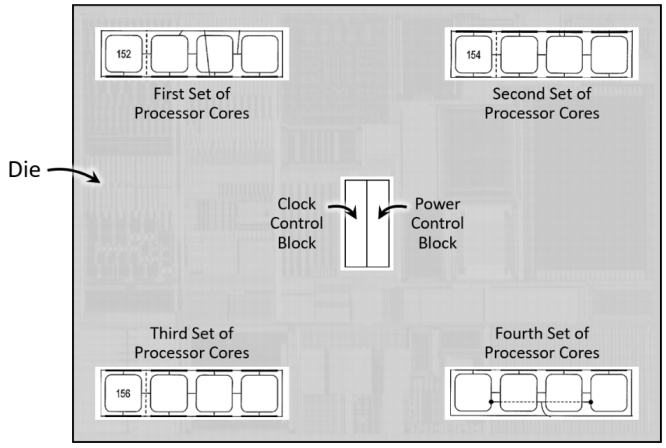
'339 Patent Claim(s)	Redstone's Proposed Construction	Defendants' Proposed Construction
Claim 14	Plain and ordinary meaning	Indefinite

The term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is indefinite because it fails to inform a POSITA, with reasonable certainty, both (1) when a component is "located in a common region," or not, and (2) when the "region" is "substantially central to the first set of processor cores and the second set of processor cores," or not. *See Nautilus*, 572 U.S. at 901 (requiring "reasonable certainty").

Beginning with the second ambiguity identified above, claim 14 requires "control blocks located . . . substantially central" to the sets of processor cores. "[S]ubstantially central" is a term of degree that, in the context of the '339 Patent's claims and specification, "fails to provide sufficient notice of its scope." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) ("As we have explained, a term of degree fails to provide sufficient notice of its scope if it depends 'on the unpredictable vagaries of any one person's opinion.'" (citation omitted)).

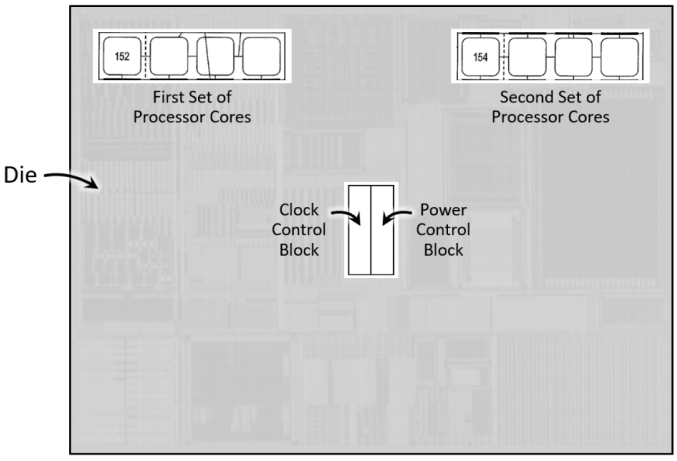
Looking first at the claims, independent claim 1 and dependent claim 14 provide no physical requirement for the individual processor cores of the claimed multi-core processor. As noted above in Section IV.B, one skilled in the art understands that the components of a multi-core processor may be located throughout the semiconductor die upon which they are typically formed; the processor cores need not be immediately adjacent in the manner shown in Figure 1 of the '339 Patent. *See also* Villasenor Decl. at ¶¶ 69-70. The below figure depicts one possible physical layout of the multi-core processor of the claims, with the sets of processor cores from '339 Patent Figure 1

placed towards the corners of the semiconductor die and the control blocks at the midpoint between the sets of processor cores:



Villasenor Decl., Figure H.

Even in such an arrangement, a POSITA would not know whether the control blocks are "substantially central" by virtue of being equidistant from each set of cores, or whether the control blocks are not substantially central given the separation of the processor cores from the control blocks. *Id.* at ¶ 85. The uncertainty within "substantially central" becomes more pronounced, however, if only two sets of processor cores are considered—as in the Asserted Claims. The figure below depicts the first and second sets of processor cores at the top of the die with control blocks near the middle:



Id., Figure I.

A person skilled in the art would not know in the context of claim 14 whether (a) the depicted control blocks are "substantially central" because they are at the horizontal midpoint between the first and second sets of processor cores, or (b) whether the control blocks are not "substantially central" because they are not in the same vertical position as the sets of processor cores. *Id.* at ¶¶ 87, 88.

The specification of the '339 Patent similarly provides no guidance regarding the scope of "substantially central." *See Interval Licensing*, 766 F.3d at 1371 ("Where, as here, we are faced with a 'purely subjective' claim phrase, we must look to the written description for guidance." (citation omitted)). The term "central" and the phrase "substantially central" are never used in the patent's specification. And, while the term "substantially" appears twice, neither use concerns the physical relationship between control blocks and processor cores. *See* '339 Patent at 4:24-27 (denoting commonality between Figs. 3 and 4), 6:56-57 (providing boilerplate regarding "the use of substantially any plural and/or singular terms herein.").

Because claims 1 and 14, and the patent's specification, do not require a physical arrangement of the sets of processor cores, a person skilled in the art could not determine with reasonable certainty whether or not "control blocks" are "substantially central" to the sets of processing cores. "[L]ocated in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is therefore indefinite.

An independent ground for indefiniteness arises from claim 14's use of "common region." Claim 14 requires "the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a ***common region***." Though not a model of clarity, a POSITA understands this phrase means the

first and second sets of processor cores share a common region where control blocks are located. *See* Villasenor Decl. at ¶ 79. The claims provide no indication, however, of what constitutes a "region" corresponding to a set of processor cores or how such regions could be in "common." *Id.* at ¶¶ 80-81.

While one possible interpretation of a common region shared by first and second sets of processor cores could be that the sets of processor cores "overlap" in physical space, this interpretation conflicts with dependent claim 9, which depends from claims 1 and 8. Claim 9 (through its dependencies) requires a "first set of processor cores [] located in a first region," a "second set of processor cores [] located in a second region," and "the first region and the second region are overlapping regions." When construing claims, "[d]ifferent claim terms are presumed to have different meanings." *SimpleAir, Inc. v. Sony Ericsson Mobile Communs. AB*, 820 F.3d 419, 431 (Fed. Cir. 2016) (citing *Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008)). Therefore, "common region" in claim 14 must mean something other than overlapping, though such other meaning remains unclear. *See* Villasenor Decl. at ¶ 81.

The '339 Patent's specification does not resolve the ambiguity introduced by "common region" in claim 14. The patent's specification never uses the phrase "common region." And, while the specification describes an embodiment with two control blocks "arranged in a common area," that use is distinct from claim 14; there is no reference in the specification to sets of processor cores sharing a "common area." *Id.* at ¶ 82.

The phrase "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is indefinite for two independent reasons: a POSITA cannot determine with reasonable certainty the scope of each of "common region" and "substantially central."

V. CONCLUSION

For the foregoing reasons, Defendants respectfully request the Court construe Term 1 as proposed by Defendants and find Terms 2 and 3 indefinite as set forth herein.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was served on counsel of record via the Court's electronic filing system on April 4, 2025.

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